Multichip IMPATT Power Combining, a Summary with New Analytical and Experimental Results

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Abstract—*X* band IMPATT diode chips have been efficiently combined in parallel, in series on diamond heat sinks, and in series–parallel on diamond heat sinks. This paper summarizes experimental and analytical work performed over a four-year period and places some of the results in perspective with respect to practical applications. Several device types have shown to be compatible with series geometries. Analysis has shown that some device types, when connected in series, form a combination which is neither open-circuit nor short-circuit stable, an intrinsically unstable condition. It has been shown further that capacitors of practical size can be placed in parallel with each chip of such an assembly to prevent the occurrence of the unstable condition. Thus unique problems reported earlier [1] with some types of IMPATT's are understood and can be prevented. These experimental and analytical results appear to eliminate any hypothetical barrier to the routine series power combining of at least several types of IMPATT device chips.

I. Introduction

EXPERIMENTS with various IMPATT diode chips have provided data which show that IMPATT chips can be efficiently combined in a variety of multichip configurations if certain instabilities are eliminated. *X*-band assemblies have been configured in series-on-diamond, in parallel, in series–parallel-on-diamond and using lumped circuit elements. Several device types (Table I) have been combined efficiently (90 percent or higher) and stably (no spurious modes) in one or more of the configurations, but not all combine readily with the same approach or with equal ease. With GaAs-device chips, the inherent chip parameter variations within a batch do not constitute an inordinate problem, but modification of the multichip configurations is required in some instances to accommodate batch-to-batch variations. The more efficient devices are oftentimes somewhat difficult to combine. Silicon CW p^+-n-n^+ chips (efficiency$\approx$5–8 percent) are an exception to this observation and combine in series only with great difficulty.

Multiple mesa IMPATT chips, wherein all the mesas are connected in parallel in a microwave package, have been used by many diode manufacturers and are not discussed herein. Some interesting experiments with this type of device were reported earlier [2]. A multichip IMPATT consists of two or more separate IMPATT chips connected in some compact way to achieve stable oscillation or amplification with higher power output and high combining efficiency. Primary emphasis has been with chips connected electrically in series-on-diamond. Fig. 1 shows several possible geometries for such devices. Early experiments were performed using two silicon IMPATT chips on a single diamond heat sink mounted in a conven-

TABLE I
TYPES OF IMPATT CHIPS AND SUPPLIERS

TYPE OF CHIP	SOURCE
C.W. SILICON P^+-N-N^+	GEORGIA TECH
C.W. GAAS SCHOTTKY LO-HI-LO	RAYTHEON
PULSED GAAS P^+-HI-LO	VARIAN
PULSED GAAS DOUBLE-DRIFT	RAYTHEON

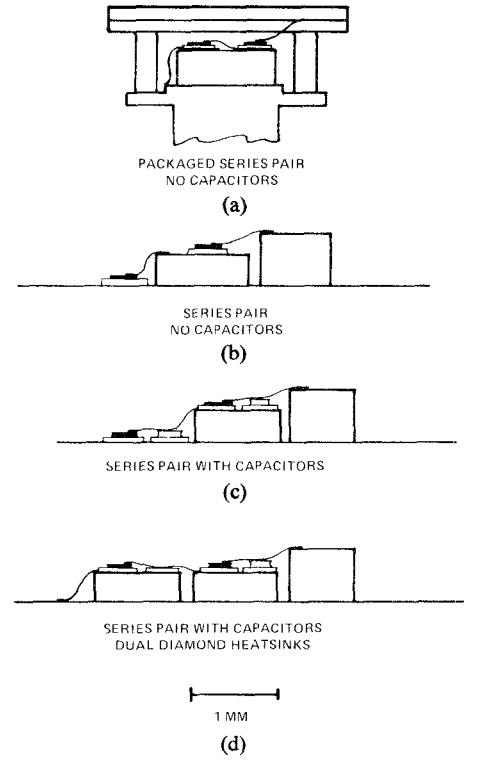

Fig. 1. Possible multichip geometries.

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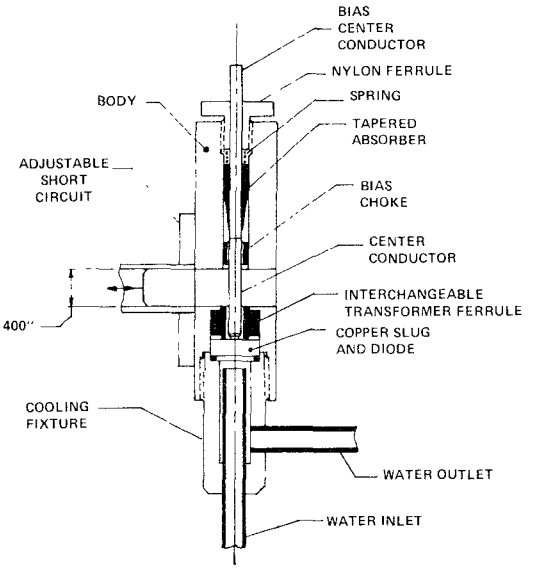


Fig. 2. RF test fixture.

tional diode package, as shown in the upper sketch (a). Other experiments used the unpackaged configurations of sketch (b). Neither of these arrangements provided stable addition of the respective chip powers except at very low current density. To correct this problem, quartz capacitors were placed in parallel with each diode chip as shown by sketches (c) and (d). Both (c) and (d) allowed stable maximum power operation as explained elsewhere herein.

All the devices have been constructed on copper slugs and tested in the RF fixture of Fig. 2. Slugs having 0.500-in and 0.200-in diameter have been used with equal performance.

II. Problems/Stability

With the foregoing details of geometry and fixture as a starting point, it is judicious to note that approximately a year of effort was expended before the first efficient full power series IMPATT assembly was achieved, Josenhan's [3] earlier three-chip demonstration notwithstanding. Attempts to duplicate his exact diamond-device geometry using available silicon flat profile chips failed.

The most severe problems encountered during these early experiments were instability and power saturation at low current levels with the series connected silicon chips. Numerous tests on these devices without parallel capacitors resulted in what appeared to be relaxation-type oscillations at frequencies from approximately 1 to 4 GHz for low dc current levels. Although a single chip would operate well when biased to over 100 mA, a series pair would become unstable at current levels of 30–40 mA. Statistically, the data of these tests showed a "probable" linear relationship between the frequency of spurious oscillations and the square root of the current density at which instabilities occurred. This behavior tended to relate the instability of one chip to possible parametric effects associated with the avalanche resonance of another chip. This led to a working hypothesis that instabilities occurred in series-connected devices when the avalanche processes of one chip, acting alone or with other circuit elements, provided a parallel resonance for the other chip(s) at or near a subharmonic of the operating frequency.

Other experiments were devised as further tests of this hypothesis. It was reasoned that if the instability of one chip was caused by a resonance associated with the avalanche processes of another chip, it should be possible to increase the current level at which breakup occurred by intentionally adding capacitance directly in parallel with each individual chip. By so doing, the troublesome resonance would be tuned to a lower frequency for a given dc current; the net result being that higher currents could be reached before the resulting resonance approached the same subharmonic at which instability occurred without the capacitors. The improved results obtained by adding parallel capacitance across each chip strongly supported the hypothesis that the instability was somehow related to the avalanche resonance.

Surprisingly, the first experiments with series-connected high-efficiency GaAs chips did not exhibit the same low current instabilities that were consistently observed with the silicon chips. This later proved to be the case with various other GaAs Schottky and p-n junction devices having both hi–lo and lo–hi–lo doping profiles. These results prompted further theoretical studies which dealt with basic device differences and the implication on circuit stability.

The measured small-signal impedances of high-efficiency (hi–lo and lo–hi–lo) GaAs devices were found to differ from those of Si devices in two respects.

1) At high bias currents, the reactance of some GaAs chips was capacitive even down to 200 MHz (the low-frequency limit of the analyzer) while the Si chips exhibited well-defined resonance.

2) At low-bias currents, the GaAs chips exhibited a resonant frequency below the cutoff frequency[1] opposite to that generally observed for silicon chips.

The manner in which the actual devices differed, especially about the "resonant" or avalanche frequency, is best illustrated by the small-signal admittance plots shown in Figs. 3 and 4. These plots, obtained by reducing network analyzer data to chip admittances, are for CW silicon p^+-n-n^+ and GaAs Schottky lo–hi–lo devices used in most of the CW series combining experiments. Also shown are calculated curves generated from a modified Read diode model whose parameters were chosen to obtain a "best fit" to the measured chip data for bias currents of 25 and 100 mA. The curves are based on a diode model [4] in which the avalanche, or natural reso-

[1]The terms "resonant frequency" and "cutoff frequency" are taken from *Physics of Semiconductor Devices*, by S. M. Sze in which the resonant frequency f_r is defined to be "that frequency at which the imaginary part (B) of the admittance changes from inductive to capacitive," and the cutoff frequency f_c is defined to be "the minimum frequency at which the real part of the admittance changes from positive to negative." Sze further states that "For a Read diode, f_c is exactly equal to f_r. For a general IMPATT diode, it will be shown, however, that f_c is lower than f_r, and that as the avalanche width increases, the difference becomes larger." The admittance behavior observed for the GaAs devices is in contradiction with the last statement.

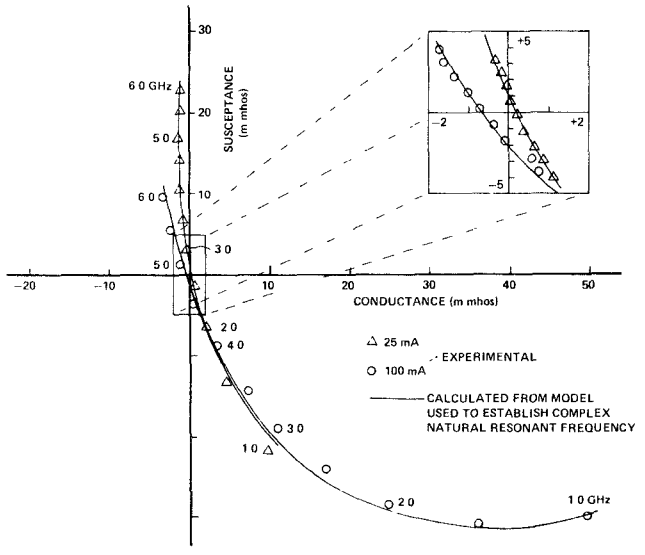


Fig. 3. Small-signal admittance of silicon p^+-n-n^+ device.

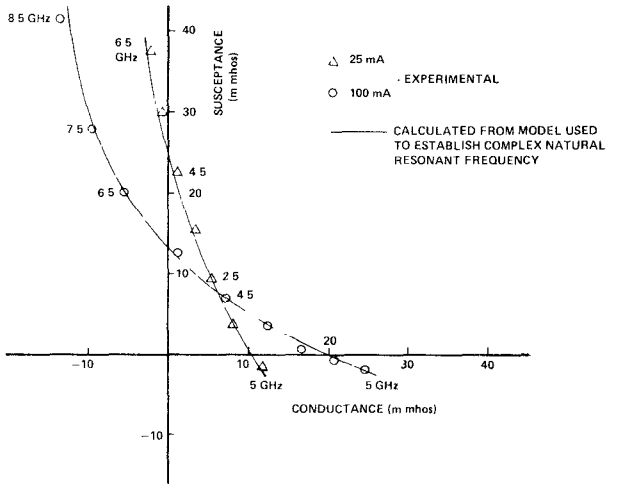


Fig. 4. Small-signal admittance of GaAs lo–hi–lo device.

nant, frequency is allowed to be complex (equivalent to including positive and negative resistive elements in the equivalent circuit of the avalanche zone). The admittance curves do not, in general, pass through zero as would those generated from a true Read model. The modified model included resistive elements in the avalanche zone equivalent circuit to simulate the effects of space charge, saturation current, unequal ionization coefficients and velocities, etc. Phenomenologically, finite saturation currents introduce positive damping to the avalanche processes, whereas space charge feedback effects usually introduce negative damping or a negative differential resistance. These effects were modeled, respectively, as a positive resistor in series with the usual avalanche inductor and a negative conductance in parallel with the combination.

Fig. 5 is a plot of the complex natural resonant frequency (the pole, $s_a = \sigma_a + j\omega_a$, of the device impedance) obtained for each device by curve fitting the experimental data at the various dc bias currents. The real part of the complex frequency σ_a can be approximated by a negative

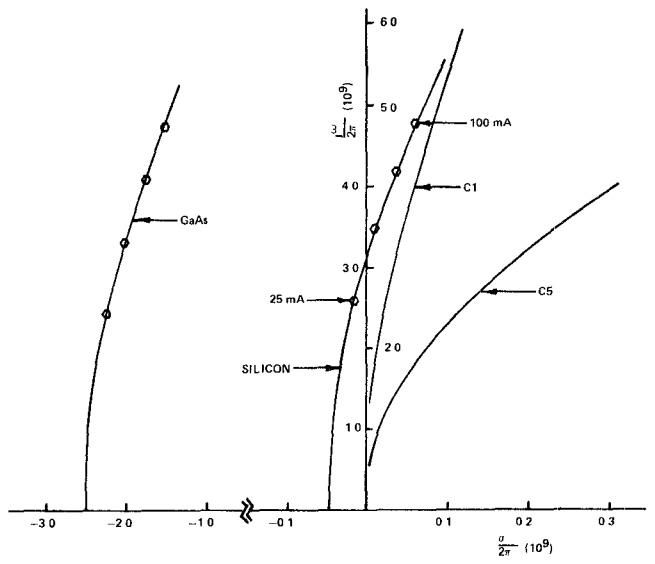


Fig. 5. Locus of natural resonant frequency for GaAs and Si devices. Note scale change for GaAs device. ($C1$ and $C5$ after Gummel and Scharfetter [6].

term (corresponding to positive damping) which is independent of current and a positive term (corresponding to negative damping) which is directly proportional to bias current, i.e., $\sigma_a = -k_1 + k_2 I$ where k_1 and k_2 were chosen to fit the experimental data. The imaginary part is directly proportional to the square root of bias current and, of course, corresponds to the well-known avalanche frequency.

The circuit model used to fit the data is identical to that described by Hulin [4] *et al.*, and Goedbloed [5]. It is also consistent with that of Gummel and Scharfetter [6] who described the avalanche region of an IMPATT device by a complex function F, the poles of which correspond to its complex natural resonant frequency. The locus of the poles for their idealized diodes $C1$ and $C5$ are also shown in Fig. 5. These poles were calculated assuming zero-saturation current, hence they lie within the right half of the complex frequency plane (RHP). The effective avalanche widths of 1 and 5 μm, respectively, bracket the estimated value of 2.0 μm for the silicon chip used here.

The plots of Fig. 5 are typical of a large number of devices measured. As seen, there is a significant difference between the complex natural resonant frequency (or pole in device impedance) of the silicon device and that of the GaAs device. The natural resonant frequency (hereafter referred to as pole) of the silicon chip enters the RHP for currents greater than about 30–40 mA. In contrast, the pole of the GaAs chip remains far from the RHP for all realistic currents. It is this difference that relates directly to the relative stability of the two devices.

For example, it is well known that when the zeros or poles of a two-terminal network lie in the RHP, then the network is short-circuited or open-circuited unstable, respectively. Consider the single-chip circuit depicted in Fig. 6(a) where the load impedance has been adjusted to give a zero in total impedance at the operating frequency ($s_0 = j\omega_0$) for a bias current of 50 mA. When the bias current is

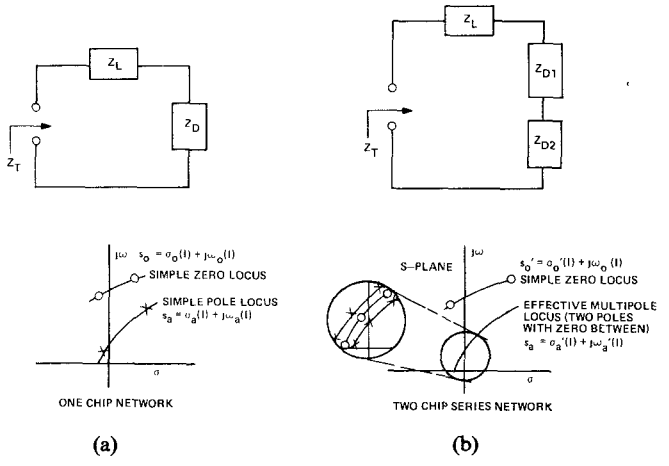


Fig. 6. Oscillator network used to illustrate instability problems of series-connected chips.

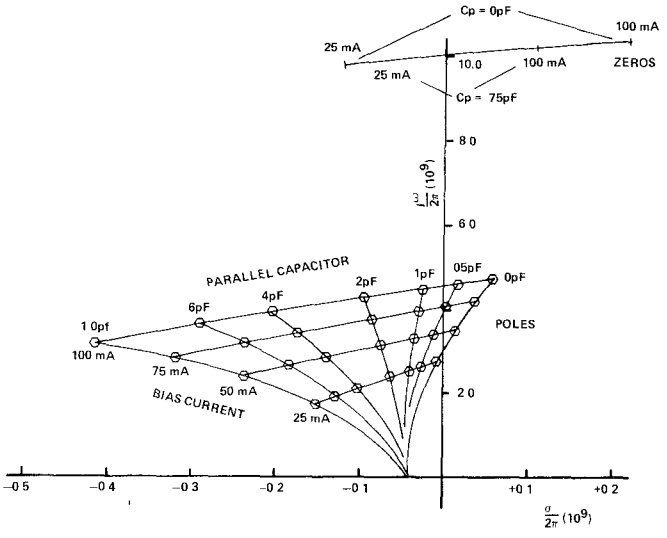


Fig. 7. Effect of parallel capacitance on locus of poles of network.

increased to 50 mA, the short-circuited network (shorted at the indicated terminals) would start oscillating at the frequency ω_0. The pole, which enters the RHP at a slightly lower current, would cause instabilities *only* if the network were open-circuited (or nearly so) at the frequency ω_a. Normal IMPATT oscillator circuits and their associated bias arrangements offer sufficiently low circuit impedance to prevent this single-chip instability at ω_a. On the other hand, consider the network depicted in Fig. 6(b), consisting of a load and two series-connected chips. One chip now provides the open-circuit for the other chip and vice versa, resulting in possible instabilities at ω_a under short-circuited conditions. In fact, the series connection of two slightly dissimilar chips results in two closely spaced poles separated by a zero which causes the circuit to be unstable when s_a enters the RHP for both open- and short-circuited conditions.

Fig. 7 shows the calculated pole-zero locus of a two-chip network in which parallel capacitors are placed across each chip. The load impedance consists of a coaxial transformer and tuning inductor whose characteristics were adjusted to maintain a zero at $s_0 = j\omega_0$ for a bias current of 50 mA as capacitance was added in parallel to each chip. As clearly illustrated, the parallel capacitors shift the locus of the poles, causing them to remain in the LHP and resulting in a stable network.

All the foregoing discussions are consistent with experiment.

1) Series-connected silicon chips of the type used become unstable at bias current levels between 30 and 40 mA.

2) The instabilities occur at approximately one third the operating frequency (initially thought to be parametric instabilities).

3) Series-connected silicon chips remain stable up to burnout only with parallel capacitors.

4) Series-connected GaAs chips of the types used are stable at current levels up to burnout.

Other calculations indicate that parallel capacitors across the individual chips greatly reduce the possibility of parametric type instabilities. Furthermore, bias circuit oscillations and related failures were considerably reduced and often eliminated entirely by use of the capacitors. These statements and observations will be expanded if possible in a forthcoming paper.

III. RF Performance

The most significant X-band results achieved were with CW GaAs Schottky lo–hi–lo and pulsed GaAs p^+-hi–lo chips. These results are summarized in Figs. 8 and 9. Each figure shows detailed SEM micrographs of typical assemblies. The accompanying graph and table include data measured on several similar assemblies. The overall size of each assembly can be estimated by noting that each of the diamond heat sinks is $\approx$0.040 sq. in. Only a small number of pulsed double-drift chips was available for tests but good results were also obtained with these chips. Table II summarizes performance obtained with the individual devices and with two devices connected in series. The feasibility established by the data of Figs. 8 and 9 was not considered sufficient proof that such performance could be repeated on a routine basis. Therefore, the improved three-chip pulsed configuration of Fig. 10 was generated. This geometry included smaller capacitors fabricated of NPO dielectric material (denoted LC-572 [$\varepsilon_r = 64$] by its supplier, Dielectric Laboratories) which allowed the output contact to be mounted on one of the diamonds thus eliminating the quartz post and permitting safe contact pressure of about 40 g.

Twelve three-chip devices were fabricated using this geometry and Varian p^+-hi–lo chips from two lots. Ten of the twelve provided $P_0 = 45$–50 W; $\eta = 16$–20 percent; and $f_0 = 10$ GHz. In two additional three-chip devices, chips from the two lots were mixed. Both devices operated efficiently but saturated at relatively low-power outputs of 34 and 43 W, respectively. Additional work is needed to prove the acceptability of mixed lot multichip assemblies.

A. Series/Parallel Pulsed Chips

Successful work with series connections of parallel pairs of CW chips (Fig. 8) led to tests of similar configurations

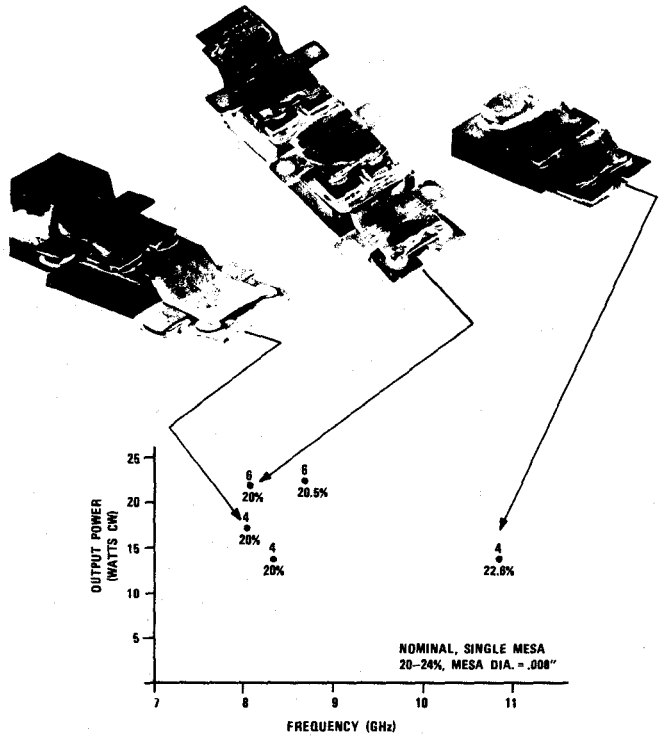
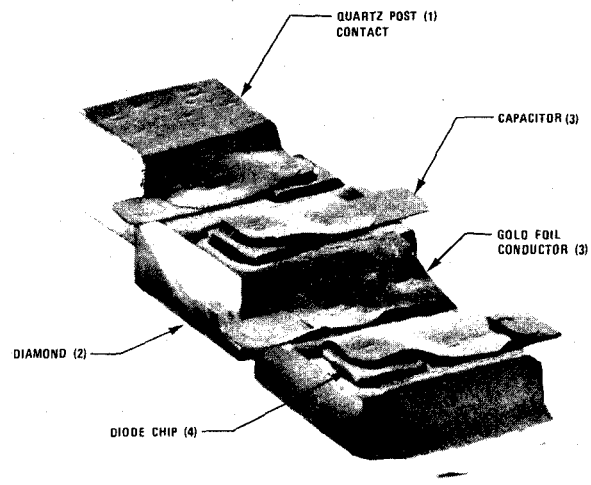


Fig. 8. RF results (CW).



No. Chips	(V) V_p	(A) I_p	(W) P_p	(W) P_o	(%) η	(GHz) f_o	(μsec) P.W.	(%) Duty
1(typical)	40/50	1.3/1.6	-	10/14	15/18	10/12	1	20
2(series)	90	1.40	126.0	21.2	16.8	11.0	1	20
	140	1.35	189.0	32.2	17.0	11.0	1	20
3(series)	150	1.43	214.5	35.1	16.4	11.0	1	20
4(series)	170	1.43	243.1	60.4	24.9	11.5	1	20

Fig. 9. RF results (pulsed).

TABLE II
PERFORMANCE WITH PULSED DOUBLE-DRIFT DIODE CHIPS

PARAMETER	SINGLE CHIP	SERIES PAIR
Po(PEAK)	15-17 W	28.5 W
EFFICIENCY	16-19 %	16-17 %
FREQUENCY	11.5-12.5 GHz	12.2 GHz

DUTY = 20%

PULSE WIDTH = 1 MICROSECOND

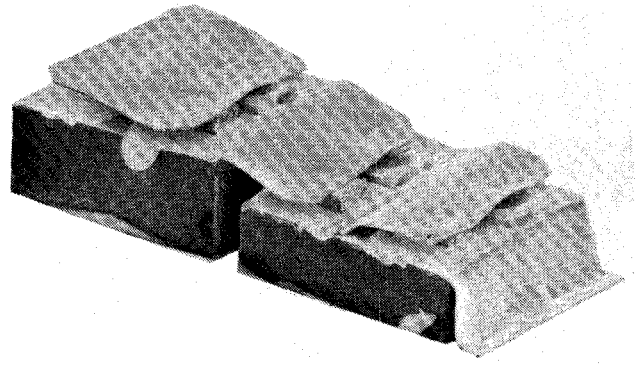


Fig. 10. Improved geometry, pulsed three-chip assembly.

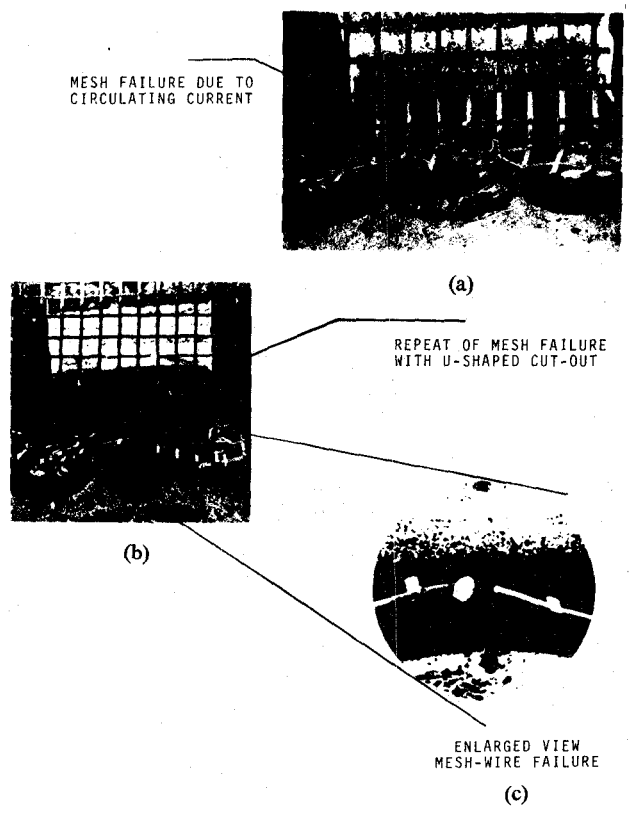


Fig. 11. Mesh failures with parallel pulsed chips.

with pulsed chips. Initial assemblies using parallel chips exhibited low efficiency and considerable tuning difficulty. One four-mesa assembly, wherein the parallel pairs of chips were connected by gold mesh, would not provide a single optimized spectral line but oscillated very weakly near 12.3 GHz prior to increasing the current to rated values. After application of rated current (3 A for parallel mesas), even these signals could no longer be obtained.

Investigation of the assembly showed that the gold mesh had melted between mesas, as shown in Fig. 11(a). The solder disc between the mesas was associated with a previous experiment and can be ignored. To insure that this failure was not a "one-time" effect, associated with explicit test conditions, the mesh was replaced as shown in Fig. 11(b). This time an inverted U-shaped portion of the mesh was removed with the exception of one mesh wire

TABLE III
PARALLEL CHIP OPERATION WITH FOIL STRAP AND 20-Ω RESISTOR

V(v)	I(A)	P(w)	P_O(W)	η(%)	F_O(GHz)	CASE
42	1.6	67.2	6.8	10.1	12.06	HEAVY FOIL STRAP
42	1.57	65.9	7.0	10.6	12.06	20 Ω RESISTOR

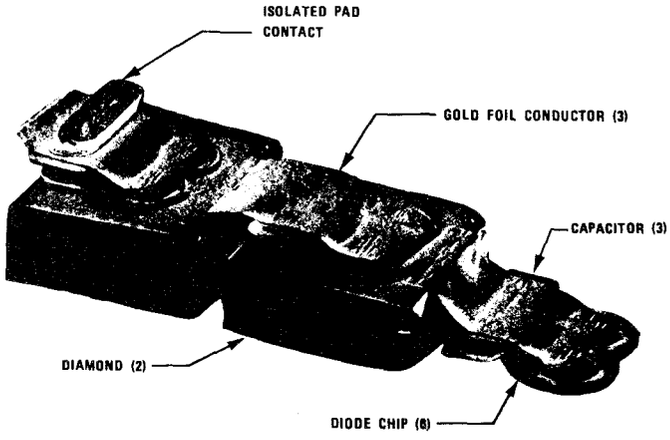


Fig. 12. Six-chip (2×3) pulsed multichip device with closely spaced parallel chips.

visible in Fig. 11(b) and enlarged in Fig. 11(c). The failure of the mesh wire is evident in both figures.

It is clear from this experiment that high circulating currents near the mesas and including the mesh were present. It is not clear whether the currents were related to the dc or RF device properties, but in view of the low-level 12.3-GHz outputs observed prior to mesh failure, a localized RF oscillation involving high RF currents, but coupled weakly to the load, seems most likely.

As a third experiment, the same two mesas were interconnected by a heavy foil strap and then by a 20-Ω resistor. Mesh was used in both cases to connect to the quartz post contact. The results in these two cases are shown in Table III. Thus although stable output was achieved, it appeared that a circulating mode, incapable of burning out either the strap or resistor but at the same frequency as the output, may have been present, resulting in the low efficiency.

To test this possibility, a two-mesa device was fabricated with less than one-mesa diameter spacing (the heat sinks were trimmed to allow close spacing). This parallel pair operated efficiently, apparently without circulating currents.

Subsequently, six 3.1-pF device chips were selected and assembled using close spacing. The resulting six-chip assembly (Fig. 12) provided the highest peak power (53.2 W) obtained using the series–parallel geometry. The overall performance of this assembly was that given by Table IV.

The four-mesa series configuration of Fig. 9 provided higher peak power (60 W) with only four chips. Some of this difference can be explained by differences in chip area. The series four-mesa configuration employed 4.0-pF chips as compared to the 3.1-pF chips used in the

TABLE IV
RF PERFORMANCE, SIX-CHIP PULSED SERIES–PARALLEL DEVICE

V(v)	I(A)	P(w)	P_O(w)	η(%)	F_O(GHz)	DUTY
140	2.27	317.8	53.2	16.7	10.46	20%

series–parallel assembly above. The series–parallel assembly would be expected to provide about 69 W using 4.0-pF chips if the 16.7-percent efficiency did not change. Well-matched chips of this size were not available for further experiments; therefore, neither device area nor the efficiency differences noted could be explored further.

IV. INJECTION LOCKING

Rudimentary injection-locking experiments were performed on single-chip and three-chip devices. The locking bandwidth and power variation are given by Figs. 13 and 14 which are self-explanatory. These data are rudimentary in that each device was simply placed in the fixture of Fig. 2, adjusted for maximum power, and tested; no effort was made to optimize the bandwidth in either case. The data clearly show, however, that no unique problem exists with respect to the multichip device. The output spectrum faithfully reproduced that of the input signal over at least ±100-MHz bandwidth.

V. MULTICHIP ASSEMBLY

All multichip assemblies were fabricated using relatively standard semiconductor laboratory tooling and equipment. Fig. 15 is a sketch of the four-chip 60-W pulsed diode of Fig. 9. The device is typical and was prepared and assembled in the manner described below.

1) The 1-mm square×0.5-mm thick diamond heat sinks were cleaned and metallized, top and bottom, with 0.07 μm of evaporated chromium followed by 0.2 μm of evaporated gold. The gold was followed by an additional 4 μm of electroplated gold.

2) The diamonds were next mounted on a glass slide and masked using black wax to obtain the desired separate metallized pads evident on the top surface of each diamond. This step also removed residual metallization unavoidably deposited on the sides of the diamond heat sinks.

3) The diamond heat sinks were then compression bonded to a gold-plated annealed copper slug using a diamond-tipped bonding stylus. Pressure of 25 kpsi and temperature of 300°C were used. In some instances, a somewhat higher pressure was used to press the diamond part way into the copper slug. The lower right-hand heat sink of Fig. 15 has been treated in this manner.

4) Next, the stabilization capacitors were compression bonded at 300°C and 15 kpsi and the quartz contact post was soldered or compression bonded in place.

5) Prior to final assembly, the diode chips were soldered in place using an induction heated collar and 80/20 Au–Sn solder at 280°C. Since each diode required a separate solder cycle, the cycle length (time at solder

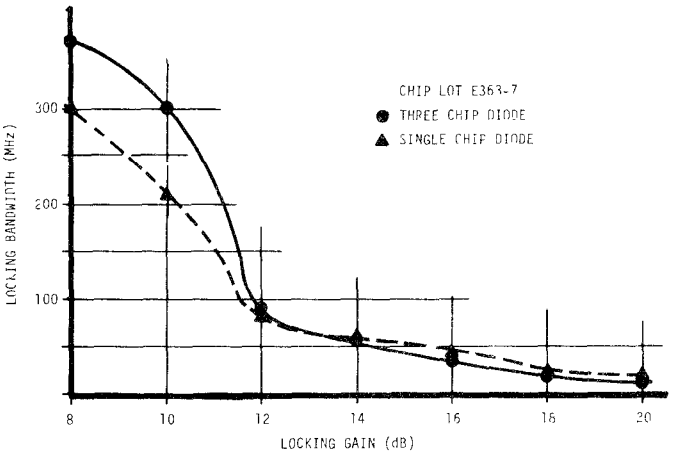


Fig. 13. Injection-locking bandwidth, single-chip and three-chip pulsed IMPATT.

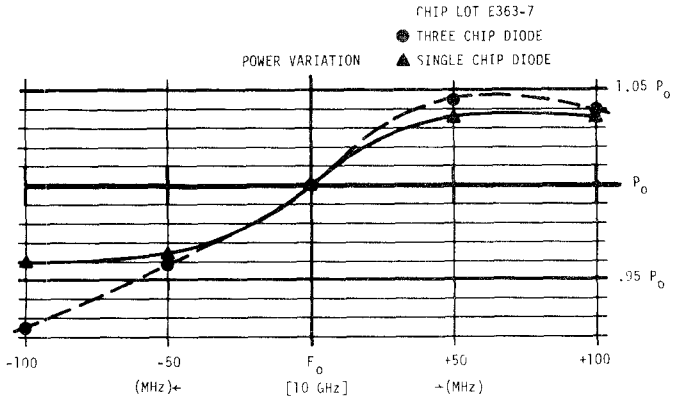


Fig. 14. Power variation over injection-locking band.

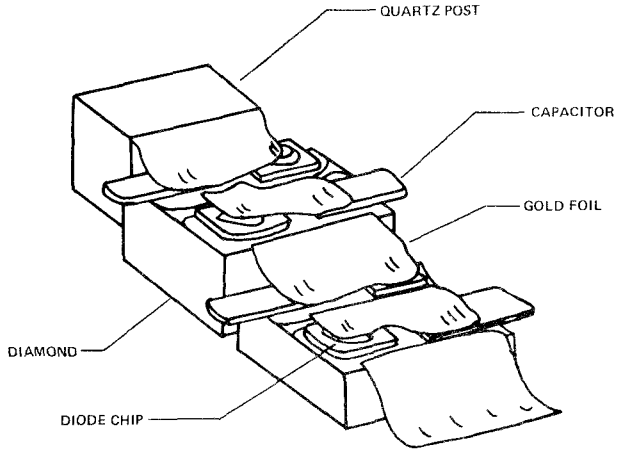


Fig. 15. Sketch, four-chip 60-W pulsed diode assembly.

temperature) was minimized so as to prevent damage to previously soldered chips. The cycle was terminated by injection of hydrogen as a rapid-cool gas.

6) As a final step, gold foil was cut to the desired dimensions and compression bonded at 275°C utilizing a sapphire bonding wedge.

The foregoing process is tedious and requires considerable skill. Given the large number of devices and multichip geometries fabricated, it was not practical to use jigs, fixtures, and photolithography to simplify metallization and assembly. The diode chips were used as received from the vendors. The chips were of the plated heat-sink type and required solder bonding. Therefore, other mounting means, such as thermocompression bonding, could not be used to mount the chips. Finally, the interconnections, chip-to-chip, could be simplified by use of a beam-leaded approach. Diodes having beam leads were unavailable.

VI. Conclusions

Several IMPATT chip types have been successfully combined in series on diamond to provide n-fold power increase at X-band frequencies. Methods of insuring the stability of such series-combined assemblies have been determined and analyzed. The techniques used have been applied to a large enough sample lot to demonstrate both repeatability and practicality.

Acknowledgment

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